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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/303,669	05/03/1999	STEFANOS SIDIROPOULOS	RMBS.002	8670

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EXAMINER	
FAN, CHIEH M	

ART UNIT	PAPER NUMBER
2634	

DATE MAILED: 11/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/303,669	SIDIROPOULOS, STEFANOS	
	Examiner	Art Unit	
	Chieh M Fan	2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 January 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *5-7,12-15,17-25,30 and 31* is/are allowed.

6)☒ Claim(s) *1-4,10,11 and 26-29* is/are rejected.

7)☒ Claim(s) *8,9 and 16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/01122004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

2. Claims 1, 26 and 27 are rejected under 35 U.S.C. 102(e) as being anticipated by Tamura et al. (US Patent 6,247,138, "Tamura" hereinafter).

Regarding claim **1**, Tamura discloses a clock alignment circuit comprising:

a delay line having a plurality of delay elements (311 in Fig. 44), wherein each delay element of the plurality of delay elements includes a supply electrode to receive a supply voltage ("CS" input to 311 in Fig. 44, also see Fig. 45 for the details of each of the delay element "D", also note that "CS" is a control voltage, see bottom of Fig. 45), to

generate a delayed clock signal ("CKin" in Fig. 44) with respect to a reference clock signal ("CKr" in Fig. 44);

a comparator (312 in Fig. 44), coupled to the delay line, to compare the delayed clock signal and the reference clock signal and to output delay differential information ("UP" and "DN" output from 312 in Fig. 44), wherein the delay differential information is representative of a correction information between the reference clock signal and the delayed clock signal;

charge pump circuitry (131 in Fig. 44), coupled to the comparator, to convert the delay differential information to a control signal ("Vco" output from 131 in Fig. 44), wherein the control signal is proportional to the delay differential information;

an amplifier (132 in Fig. 44) coupled to the charge pump circuitry, wherein the amplifier includes:

a first input ("+" terminal of 132 in Fig. 44) to receive the control signal;

a second input ("-" terminal of 132 in Fig. 44) to receive a feedback signal; and

an output (output of 132 in Fig. 44) to provide the supply voltage and the feedback signal responsive to the control signal.

Regarding claim **26**, Tamura discloses a method of generating a supply voltage ("CS" in Fig. 44, note that CS is a control voltage, see bottom of Fig. 45) for use in clock compensation circuitry (301 in Fig. 44), the clock compensation circuitry includes a plurality of delay elements in a delay line (311 in Fig. 4) and receives a clock signal ("CKr" in Fig. 44), the method comprising:

providing a supply voltage to a common source electrode of the plurality of delay elements ("CS" input to 311 in Fig. 44, also see Fig. 49 for the details of each of the delay element "D"; Fig. 49 clearly shows providing control voltages Vcp and Vcn to the sources of the CMOS inverter DI);

providing a delayed clock signal using the delay line ("CKin" in Fig. 44) , the delayed clock signal having a time delay with respect to the clock signal (as shown in Fig. 44, "CKin" is obtained by delaying "CKr");

detecting a delay skew between the delayed clock signal and the clock signal (312 in Fig. 44);

converting the delay skew to a voltage signal wherein the voltage signal is proportional to the delay skew (131 in Fig. 44, especially "Vco" output from 131 in Fig. 44); and

generating the supply voltage ("CS" in Fig. 44) by an amplifier (132 in Fig. 44) responsive to the voltage signal.

Regarding claim **27**, Tamura also teaches that the delayed clock signal ("CKin" in Fig. 44) is provided by propagating the clock signal ("CKr" in Fig. 44) through the plurality of delay elements ("D" within 311 in Fig. 44) and tapping an output of one of the delay elements from the plurality of delay elements ("CKin" is output from the last delay element of 311 in Fig. 44).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 2-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tamura et al. (US Patent 6,247,138, "Tamura" hereinafter) in view of Hughes et al. (US Patent 5,229,668, "Hughes" hereinafter), Tomisawa (U.S. Patent No. 5,012,141) and Blomgren et al. (U.S. Patent No. 6,107,835, "Blomgren" hereinafter).

Tamura teaches the claimed invention (see the rationale applied to claim 1 above), but does not teach that each delay element is a static CMOS inverter.

However, the use of a static CMOS inverter as a delay element is well known in the art (even the applicant considers a static CMOS inverter is just a conventional delay element, see page 15, line 21 through page 16, line 1). Hughes teaches using a static CMOS inverter for each of a series of delay elements (Fig. 4A, col. 6, lines 50-51). Tomisawa teaches that the delay time of a static CMOS inverter is controlled by the voltages supplied to the sources of the p-channel MOS-FET and the n-channel MOS-FET (col. 6, lines 5-24). Blomgren teaches that a static CMOS has the advantage of low power consumption (col. 1, lines 36-37).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use static CMOS inverters as the delay elements of Tamura for the advantage of low power consumption. Note that, as taught by Tomisawa, when a static CMOS inverter is used as the delay element of Tamura, one of ordinary skill in the art would clearly recognize that that control voltage CS should be supplied to a transistor source, a load electrode source, or a pull-up transistor source as claimed in claims 2-4.

5. Claims 10 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tamura et al. (US Patent 6,247,138, "Tamura" hereinafter) in view of Sidiropoulos et al. ("A semidigital Dual Delay-Locked Loop", *IEEE Journal of Solid-State Circuits*, vol. 21, no. 11, Nov. 1997, pp. 1683-1692, provided in IDS filed on 6/28/99, PTO Paper#2).

Tamura teaches the claimed invention, as applied to claim 1 above, but fails to teach that the comparator includes a first pulse generator, a second pulse generator and a latch circuit as recited in claims 10 and 11, wherein the comparator corresponds to the comparator shown in Fig. 6 of the instant application. The first pulse generator corresponds to element 601 in Fig. 6. The second pulse generator corresponds to element 602 in Fig. 6. The latch circuit corresponds to element 603 in Fig. 6.

On the other hand, Sidiropoulos et al. discloses an identical phase comparator (see Fig. 7) with the phase comparator shown in Fig. 6 of the instant application. The phase comparator of Sidiropoulos et al. has the advantage of tolerating large duty cycle imperfections and still providing an accurate phase lock (page 1688, left column, lines

3-5). The phase comparator of Sidiropoulos et al. and the phase comparator shown in Fig. 6 of the instant application have exactly the same structure and perform the same function (i.e., phase comparison between the delayed clock signal and the reference clock signal).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the phase comparator taught by Sidiropoulos et al. in place of the phase comparator of Tamura, since the phase comparator of Sidiropoulos et al. has the advantage of tolerating large duty cycle imperfections and still providing an accurate phase lock.

6. Claims 28 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tamura et al. (US Patent 6,247,138, "Tamura" hereinafter) in view of Sidiropoulos et al. ("A semidigital Dual Delay-Locked Loop", *IEEE Journal of Solid-State Circuits*, vol. 21, no. 11, Nov. 1997, pp. 1683-1692, provided in IDS filed on 6/28/99, PTO Paper#2).

Regarding claim **28**, Tamura teaches the claimed invention (see the rationale applied to claim 26 above), but fails to teach that the step of detecting the delay skew includes the steps of generating a first pulse, generating a second pulse, setting a latch circuit using the first pulse, and resetting the latch circuit using the second pulse, wherein all steps are performed by the phase comparator shown in Fig. 6 of the instant application. The step of generating a first pulse is performed by the first pulse generator 601 in Fig. 6. The step of generating a second pulse is performed by the second pulse generator 602 in Fig. 6. The step of setting a latch circuit using the first pulse is

achieved by sending the pulse 610 to the latch circuit 603. The step of resetting the latch circuit using the second pulse is achieved by sending the pulse 611 to the latch circuit 603.

On the other hand, Sidiropoulos et al. discloses an identical phase comparator (see Fig. 7) with the phase comparator shown in Fig. 6 of the instant application. The phase comparator of Sidiropoulos et al. has the advantage of tolerating large duty cycle imperfections and still providing an accurate phase lock (page 1688, left column, lines 3-5). Since the phase comparator of Sidiropoulos et al. and the phase comparator shown in Fig. 6 of the instant application have exactly the same structure and perform the same function (i.e., phase comparison between the delayed clock signal and the clock signal), it is clear that the phase comparator of Sidiropoulos et al. performs the same steps as recited in claim 28.

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the phase comparator taught by Sidiropoulos et al. in place of the phase comparator of Tamura in view of Lai to detect a delay skew between the delayed clock signal and the clock signal, since the phase comparator of Sidiropoulos et al. has the advantage of tolerating large duty cycle imperfections and still providing an accurate phase lock.

Regarding claim **29**, Tamura teaches the claimed invention (see the rationale applied to claim 26 above), but fails to teach that the step of detecting the delay skew includes the steps of generating a first pulse, generating a second pulse, resetting a latch circuit using the first pulse, and setting the latch circuit using the second pulse,

wherein all steps are performed by the phase comparator shown in Fig. 6 of the instant application. The step of generating a first pulse is performed by the first pulse generator 602 in Fig. 6. The step of generating a second pulse is performed by the second pulse generator 601 in Fig. 6. The step of resetting a latch circuit using the first pulse is achieved by sending the pulse 611 to the latch circuit 603. The step of setting the latch circuit using the second pulse is achieved by sending the pulse 610 to the latch circuit 603.

On the other hand, Sidiropoulos et al. discloses an identical phase comparator (see Fig. 7) with the phase comparator shown in Fig. 6 of the instant application. The phase comparator of Sidiropoulos et al. has the advantage of tolerating large duty cycle imperfections and still providing an accurate phase lock (page 1688, left column, lines 3-5). Since the phase comparator of Sidiropoulos et al. and the phase comparator shown in Fig. 6 of the instant application have exactly the same structure and perform the same function (i.e., phase comparison between the delayed clock signal and the clock signal), it is clear that the phase comparator of Sidiropoulos et al. performs the same steps as recited in claim 29.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the phase comparator taught by Sidiropoulos et al. in place of the phase comparator of Tamura in view of Lai to detect a delay skew between the delayed clock signal and the clock signal, since the phase comparator of Sidiropoulos et al. has the advantage of tolerating large duty cycle imperfections and still providing an accurate phase lock.

Claim Objections

7. Claims 8 and are objected to because of the following informalities: "the fifth supply voltage" in lines 8-9 of claim 8 should be changed to --- a fifth supply voltage ---. Appropriate correction is required.

Response to Arguments

8. Applicant's arguments filed 1/12/04 with respect to claims 1 and 26 have been fully considered but they are not persuasive.

(a) With respect to claim 1, the applicant argues that the cited references do not teach the limitation "each delay element of the plurality of delay elements includes a supply electrode to receive a supply voltage".

Examiner's response --- The applicant is reminded that the examiner is entitled to give the broadest reasonable interpretation to the language of the claims. The examiner is not limited to the applicant's definition which is not specifically set forth in the claims. See *In re Tanaka et al.*, 193 USPQ 139, (CCPA) 1977. Claim 1 calls for the limitation of "a supply electrode", not a "source electrode". Tamura teaches supplying the control voltage Vcs to the gate of the transistor DT. The control voltage Vcs is therefore clearly a supply voltage to the gate. Further, since the gate is an electrode that receives a supply voltage, the gate clearly may be called a supply electrode.

(b) With respect to claim 26, the applicant argues that Tamura does not teach "providing a supply voltage to a source of a transistor in a delay element of the plurality of delay elements".

Examiner's response --- Tamura teaches that the delay element is not limited to the configuration shown in Fig. 45. The delay element may also use the configuration shown in Fig. 49. As shown in Fig. 49, the source of the pMOS in the CMOS inverter DI receives a voltage that is a function of the supply (control) voltage Vcp. The source of the nMOS in the CMOS inverter DI receives a voltage that is a function of the supply (control) voltage Vcn. Therefore, Tamura clearly teaches the claimed limitation "providing a supply voltage to a source of a transistor in a delay element of the plurality of delay elements".

9. Applicant's arguments with respect to claims 2-4 have been considered but are moot in view of the new ground(s) of rejection.

Allowable Subject Matter

10. Claims 5-7, 12-15, 17- 25, 30 and 31 are allowed. Claims 8 and 9 would be allowable if rewritten or amended to overcome the claim objections above. Claim 16 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

11. The following is a statement of reasons for the indication of allowable subject matter:

Claims 5-9 are allowable over the prior art of record because the prior art of record does not teach or suggest that the amplifier includes a current mirror load, a bias transistor, a first differential input transistor and a second differential input transistor.

Claims 12-15 are allowable over the prior art of record because the prior art of record does not teach or suggest that the charge pump circuitry includes a second current source receiving the first supply voltage, the second current source having a control electrode to receive the bias control signal, a second load transistor coupled to the first reference terminal, wherein the second load transistor responds to the first pump output; and a second input transistor coupled in series between the second current source and the second load transistor, the second input transistor responsive to a second phase input to provide a charge pump output.

Claim 16 is allowable over the prior art of record because the prior art of record does not teach or suggest that the supply voltage is provided to the multiplexer circuit and the interpolation circuit.

Claims 17-25 are allowable over the prior art of record because the prior art of record does not teach or suggest the operational amplifier includes a bias transistor biased by a bias voltage, and a bias generator to provide the bias voltage, wherein the bias generator having a first input coupled to the control signal and a second input to receive the bias voltage.

Claims 30 and 31 are allowable over the prior art of record because the prior art of record does not teach or suggest that the step of tracking the voltage signal includes amplifying a voltage differential between the first input and the second input, biasing the current source with a bias signal, and generating the supply voltage at the output, wherein the supply voltage is proportional to the voltage differential.

Conclusion

12. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chieh M Fan whose telephone number is (571) 272-3042. The examiner can normally be reached on Monday-Friday 8:00AM-5:30PM, Alternate Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on (571) 272-3056. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9306 for regular communications and (703) 872-9306 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-4750.

Chieh M Fan
Primary Examiner
Art Unit 2634

cmf
October 12, 2004